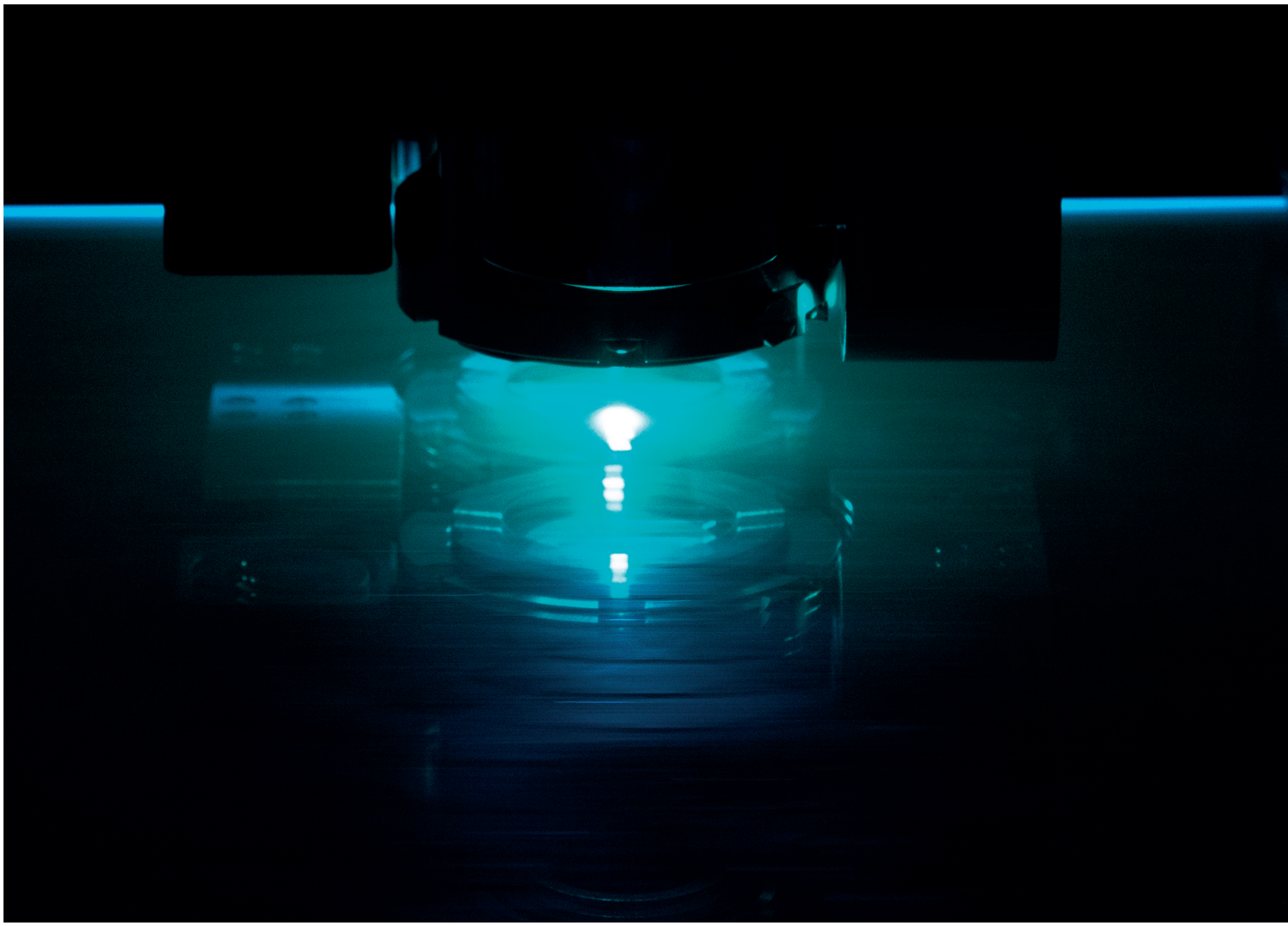
EV GROUP® | Technologies

Versatile Maskless Exposure Technology: LITHOSCALE® for Traceability in Automotive, MEMS, Photonics, Probe Cards and Advanced Packaging



Versatile Maskless Exposure Technology: LITHOSCALE® for Traceability in Automotive, MEMS, Photonics, Probe Cards and Advanced Packaging

Introduction

EVG's maskless exposure technology – LITHOSCALE® – represents a novel, digital patterning approach that enables new application development beyond the possibilities of traditional, mask–based exposure systems. The outstanding features include real-time data processing and patterning, advanced distortion function, die-shift compensation, high autofocus, high in–focus range, and top-side and bottom-side multipoint alignment capabilities.

How does the **Advanced Distortion Function** work? At first, the theoretical locations of the alignment marks are determined. After alignment marks determine **WAFER LAYOUT** positioning, the alignment marks for digital mask positioning follows. Global (4 points) and multipoint (16 points) alignment features are available. The location of the alignment marks on the wafer is measured. The layout is compensated for best match to actual wafer. The system provides the distortion of GDSII data in real time without delay. Data is distorted based on alignment information and stage distortion information to compensate for misalignment. The workflow is illustrated in Figure 1.

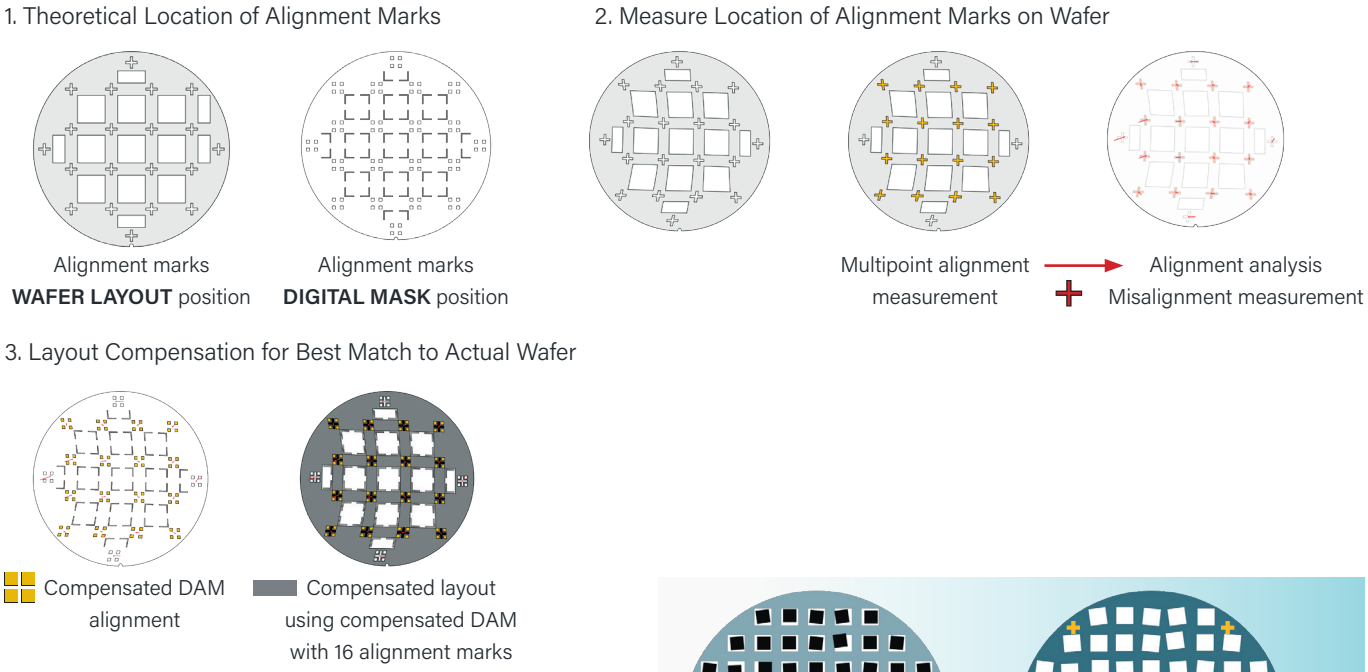


Figure 1
Schematic Process Flow of Advanced Distortion Function

Advanced distortion functionality is applied on the **DIE LEVEL**, where active compensation and re–routing results strictly rely on external metrology data. Distortion compensation algorithms include mathematical correction of rotation, scale, shear, and translation (shift). For die–placement–error compensation, the model limits distortion within the dies to the rigid body of the die, typically represented in two (external) alignment points per die. Due to the immediacy of the conversion processes, the dynamic binary pattern generation complements externally required metrology data of each die individually per substrate just before the exposure to compensate for overlay/positioning errors caused by handling or pre–processing excluding potential thermal influences. A simplified data integrity flow of die level compensation is visualized on Figure 2.

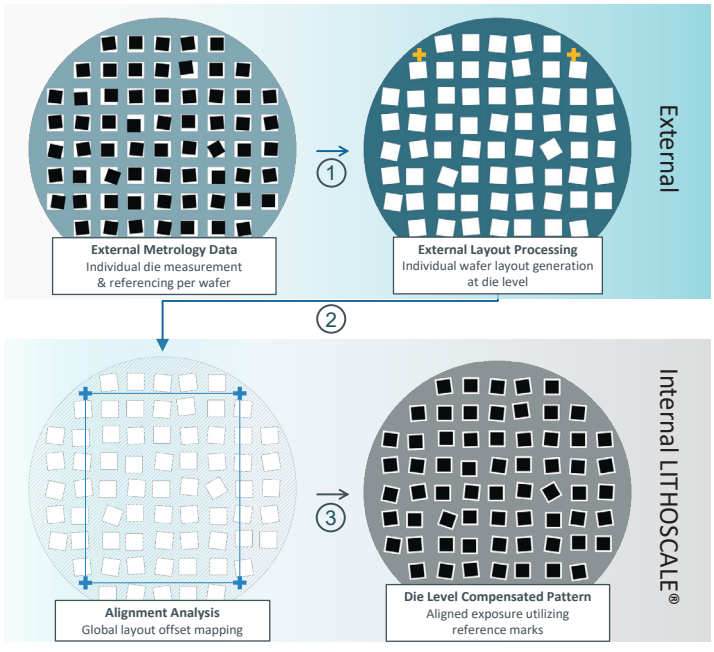


Figure 2
Schematic process flow of the die–level compensation

EVG's agile software system architectures accomplish real-time exposure. There is no additional time needed for layout conversion/calculation. There is no impact of layout flexibility on the wafer throughput.

The data processing is not limiting the throughput. The multi-head configuration enables parallel wafer processing. The minimum achieved resolution is 1.5 µm line and space (L/S). The maintenance-free **laser light source** is part of the LITHOSCALE® system. Operating with dual wavelengths, 375 nm and 405 nm, we can process a broad range of materials, including thin and thick resists, dielectric materials, and colored resists. The broad process windows matrix setup ensures efficient process evaluation.

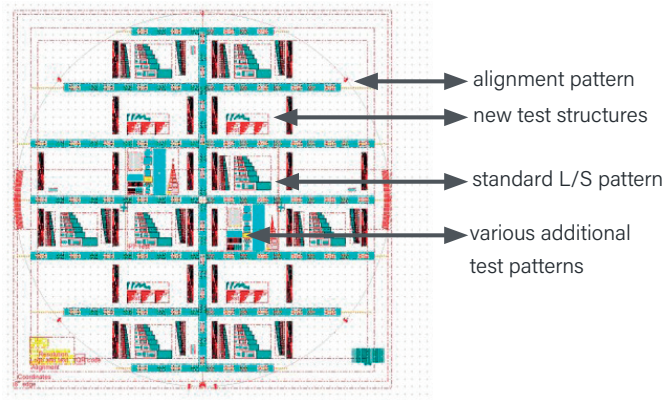


Figure 3
EVG demo evaluation resolution test GDS layout

LITHOSCALE® for Automotive Supporting Traceability Efforts in Semiconductors

Heterogeneous integration processes require the semiconductor industry to pay more attention to the tracking of manufacturing steps. Traceability efforts are especially important in automotive and medical applications. SEMI's T23 standard provides a model focusing on the minimum of key concepts, behaviors, and requirements for enabling device ID and traceability.

To facilitate the growing demand for tracking/transparency in the semiconductor supply chain, EV Group has developed the Dynamic Die Annotation as a software feature within the LITHOSCALE® maskless exposure technology. Annotations are created as templates on LITHOSCALE® and can be used in various recipes. The LotID, SubstrateID, SubstrateAquiredID, CellID, EquipmentName, ModuleName, SerialNumber, RecipeName, RecipeNamespace, ProcessJobID, ControllJobID, date, time, and year variables are applicable in recipes. Variables are replaced in real time with actual content for each wafer individually.

The onboard annotation manager includes "on-the-fly" data generation for each wafer individually. Available annotation types are Text, Codes, DataMatrix, QR Code, Aztec, PDF417, Code 39, Code 93, and Code 128. Various annotation types can be combined on one wafer. To prove the suitability of EVG's LITHOSCALE® technology for semiconductor traceability, two types of resist were used for the DataMatrix code patterning. With the positive-tone thin resist, the minimum achieved resolution is 50×50 µm for the 1 µm film thickness. In the follow-on investigation, the high-resolution negative-tone red, green and blue resists (Wave Control Materials® by FujiFilm Electronic Materials) were patterned, typically encountered in CMOS image sensor (CIS) applications. The red resist resolved readable DataMatrix Codes from 50×50 µm to 200×200 µm square for film thickness 360 nm. The green resist resolved readable DataMatrix Codes from 50×50 µm to 200×200 µm square for film thickness 310 nm. The same DataMatrix results were observed for the blue resist having FT 290 nm .

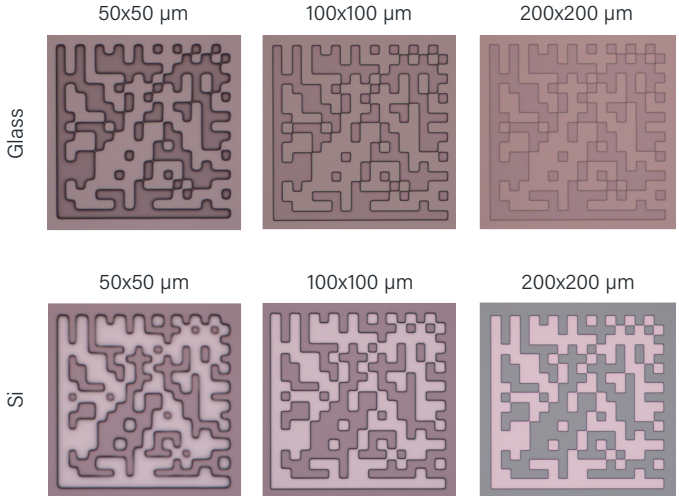


Figure 4
2D Code tests performed on glass and Si substrates by exposing data matrix codes generated by LITHOSCALE®. Smallest readable Data Matrix Code exposed is 50 µm. 2D codes can also be exposed with microscopic scale. The annotations were patterned by using AZ MiR 701, 1 µm resist thickness.*

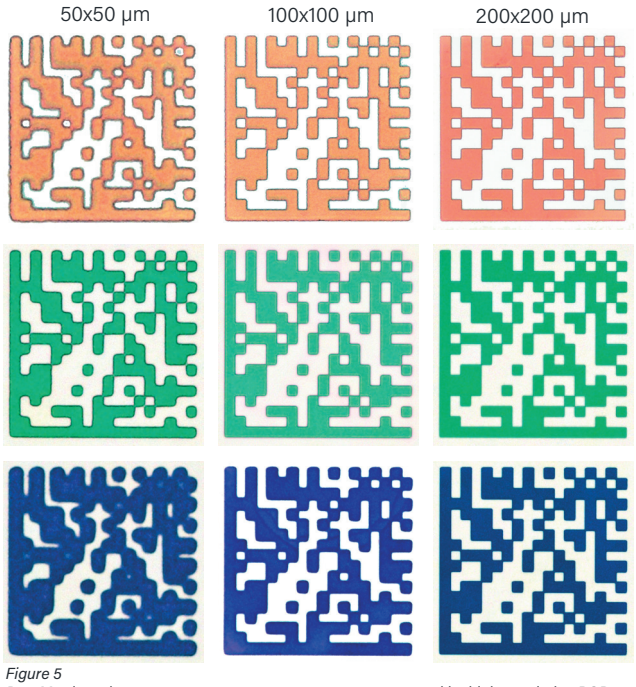


Figure 5
DataMatrix codes squares 50×50 µm to 200×200 µm patterned by high-resolution RGB resists on LITHOSCALE®.

LITHOSCALE® for MEMS and PHOTONICS

To meet the increasing demand for photonic device complexity and device optical performance, advances in lithographic patterning and materials are essential. Highly functional optical materials are getting attention in photonics for shielding and infrared (IR)-related materials. For example, wafer-level lenses are used to gather photons on the light sensitive region of CIS. To control the light transmission through the wafer lenses onto CIS, a light blocking layer is formed by applying either metal layers or the black resist. The metal layer deposition process is complex, and induces yield losses and irregular layers. The irregular light scattering resulting from defects can affect the image sensor quality. The issues related to metal deposition can be solved with LITHOSCALE® patterning of the black resist. The shielding requirements were fulfilled: reflection rate ≤2%, transmittance ≤1%, high optical density in visible range 380 – 700 nm range. The higher resolutions can be achieved vs. metal–deposition option. The applications of the LITHOSCALE® patterning with black resist include wafer–level lens shielding applications for CIS, optical projections, optical MEMS, black matrices for display, and IR shielding materials.

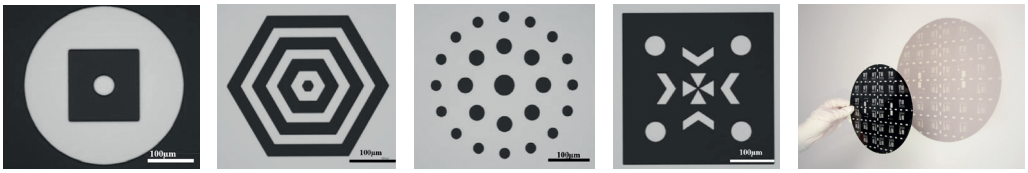


Figure 6
Flexible patterning in any arbitrary shapes. Black resist thickness between 1 – 6 µm, exposure with 375 nm.

LITHOSCALE® for FINE-PITCH PROBE CARDS

Market requirements for fine-pitch probe cards involve numerous layout designs that are unique for each new product to be tested. As a result, many masks in production are necessary, which contribute to high cost-of-ownership. Unique values of LITHOSCALE® in probe card applications include supporting immediate patterning after design release, and the ability to quickly react on end–user requests/needs and design changes. A flawless processing of the positive-tone resists and dielectric materials for fine-pitch probe cards applied in advanced NAND and DRAM memory devices is enabled. A concept of double-layer exposure is economically beneficial since the lithographic steps can be reduced when patterning the multiple RDL structures.

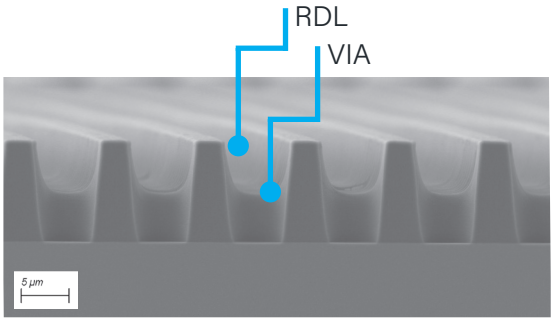
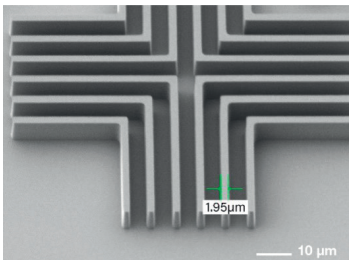


Figure 7
LITHOSCALE® dual–layer exposure of the positive tone resists for high pitch probes. The patterned RDL traces via 5 µm; opening 3 µm.



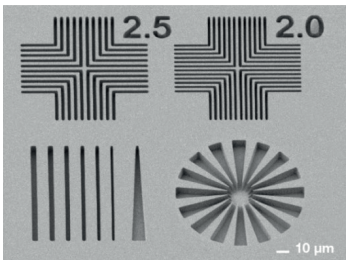


Figure 8
Baseline evaluation of L/S variation patterning performance. Positive tone thick resist, LT=8 µm. AR 4:1. Sidewall angle up to 87°.

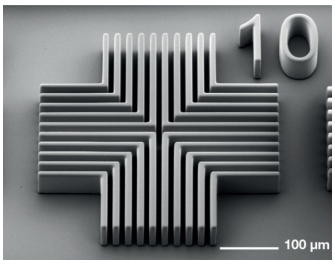


Figure 9
Thick resist, negative tone application. Layer thickness=50

LITHOSCALE® for FAN–OUT WAFER LEVEL PACKAGING for 5G, AI and HPC

The application of steppers in next–generation packaging technology is facing challenges. Accurate reconstitution of the wafers is a key parameter in integrating dies from various wafer fabs in multi–die solutions. Steppers and other mask-based patterning systems struggle to cope with inaccuracies from die-placement and die-shift variations caused by over–molding. The reticle size and optics dimensions of static exposure systems limit the exposure area. This is particularly challenging in large die interposer fabrications, where stich–lines and/or mismatches overlap regions of reticle exposure field, which can affect the electrical properties within the RDL. The ability to generate a homogenous pattern for interposers exceeding current reticle size is crucial for advanced devices needed for complex layouts, such as advanced graphic processing, 5G, AI and high-performance computing (HPC).

The solution to overcome the difficulties caused by steppers in advanced packages is EVG's LITHOSCALE® digital lithography system. Resolution and best patterning conditions of the dielectric materials were studied with LITHOSCALE®. Both negative-tone PI and positive-tone PBO formed vias with high resolution. The minimum resolution of the PI layer scales well with stress buffer layer thickness for all wavelengths studied. The effect on resolution for PBO is minimal. PBO requires a higher dose for thicker layers and resolution of PI is less dose dependent. **The proven contact via with a bottom opening down to 2 µm can significantly improve scaling and interconnect density enhancement.**

PUSHING the LIMITS of RESOLUTION

Focusing on the minimum CD for the electroplated applications, patterning of two high-performance chemically amplified resists was carried out using LITHOSCALE®, with the aim of achieving a structure size of < 2.0 µm. Several analyses of the sidewall profiles of the exposed and developed structures using SEM analysis were able to demonstrate a clear influence of the exposure wavelength, with experiments including both 375 nm, 405 nm or a combination of both. LITHOSCALE®'s digitally controlled exposure system provided a new flexible and advanced approach to fine patterning methods, applying a complete exposure matrix to narrow the process window. Accordingly, exposure dose, defocus as well as different exposure wavelengths were modulated per substrate. By combining LITHOSCALE® and Sumitomo chemically amplified materials, a resolution of 1.5 µm L/S with very high aspect ratio of up to 1:7 could be achieved without loss of throughput.

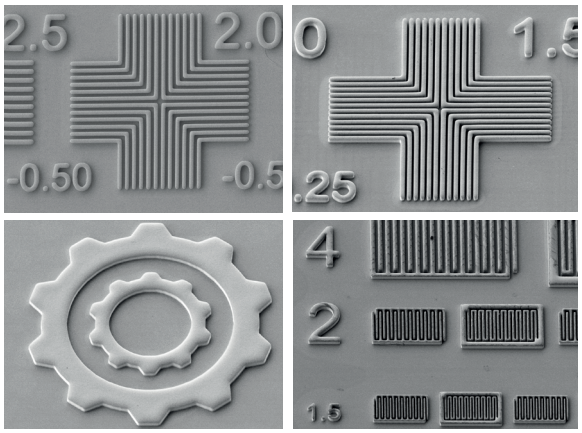


Figure 10
SEM images of Cu structures produced by electroplating: 3 µm coating thickness top view 2 µm (left) with a tilted view of 1.5 µm (right)

Figure 11
Cu structures produced by electroplating: 3 µm Cu thickness - produced utilizing Sumitomo's XI 4920 (left) and 6 µm Cu thickness - produced utilizing Sumitomo's PXI 107 (right)

Patterning of the high–resolution colored resist was conducted in the present investigation. The primary goal was downscaling feature sizes by patterning below <2 µm L/S at lower film thicknesses. Three negative-tone-colored resists, red, green, and blue, were patterned on 200 mm glass wafers. The colored resists were processed by spin coating. The wavelength 375 nm at a dose of 120 mJ/cm2 for red resist, 60 mJ/cm2 for green resist, and 45 mJ/cm2 for blue resist was employed to achieve the best patterning performance.

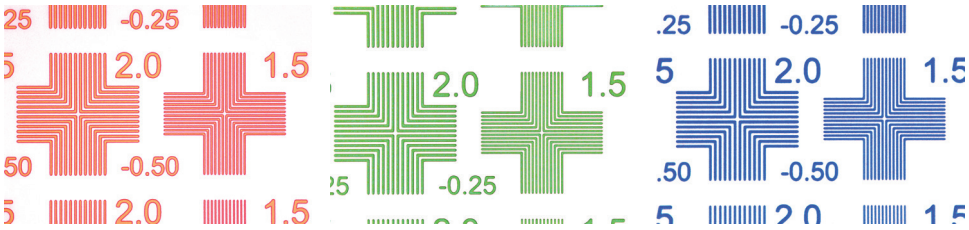


Figure 12
Optical images of the min. achieved resolution of red, green, and blue resists. Red resist FT=360nm resolution 1.5 µm L/S. Green resist FT=310 nm resolution 1.5 µm L/S. Blue resist FT=290 nm resolution 1.5 µm

SUMMARY

EVG's novel LITHOSCALE® equipment with its unique combination of mechatronics, optics and advanced software accomplishes patterning < 2 µm L/S, by efficient digital mask processing and real-time patterning.

Its distortion compensation, die-shift compensation, and alignment < 1 µm is crucial for overcoming the limitations of mask–based patterning technologies in next-generation advanced packaging devices. The technology is positioned in a variety of industries, from automotive, MEMS and photonics, to fine-pitch probe cards and more. The future of lithography technology is definitely digital.

Get in touch:

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*The white paper is a short summary of the conference papers held at ECTC, EPTC, SPIE and WLP conference.